

FIG. 1

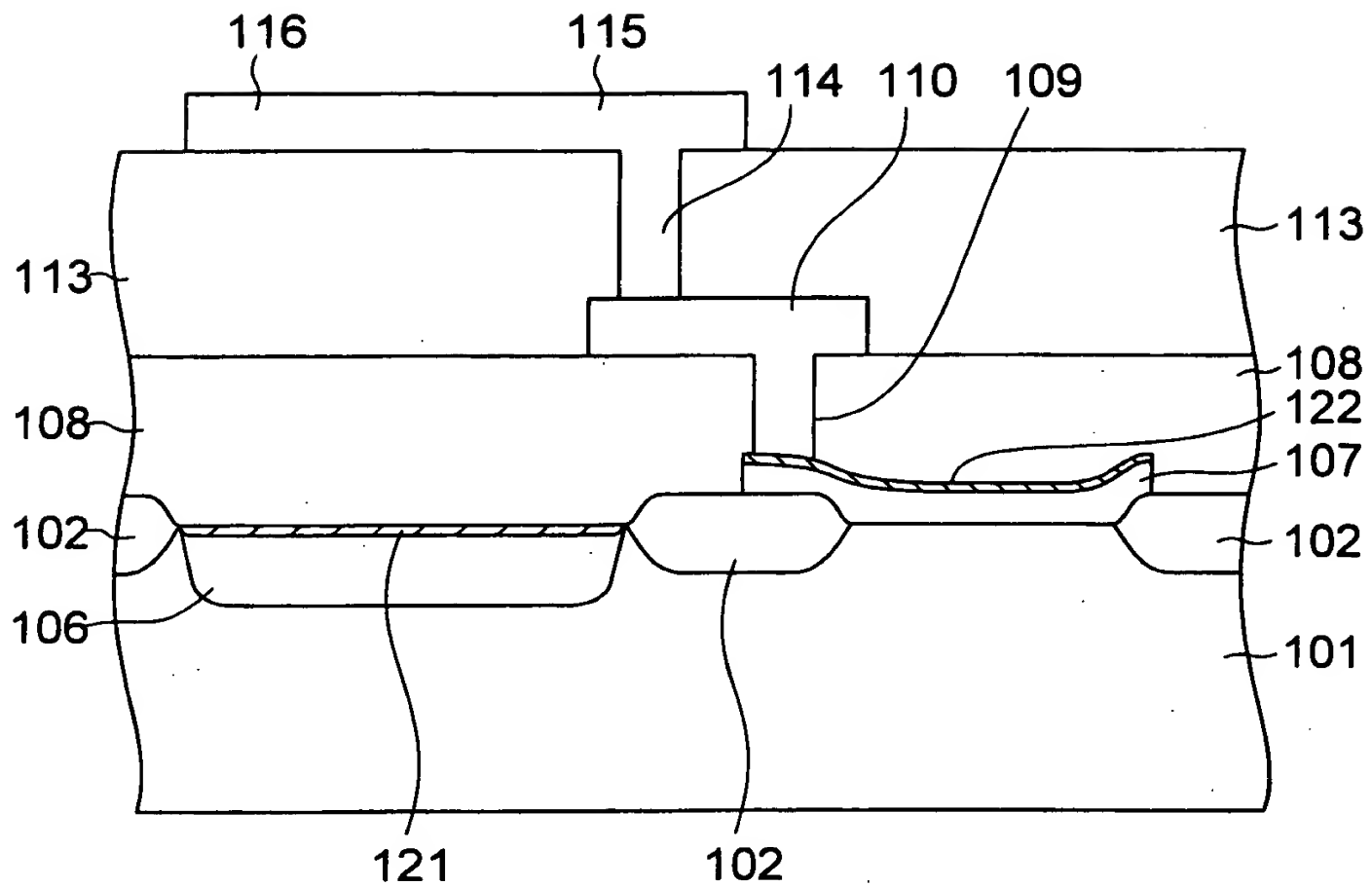


FIG. 2A a-a' SECTION

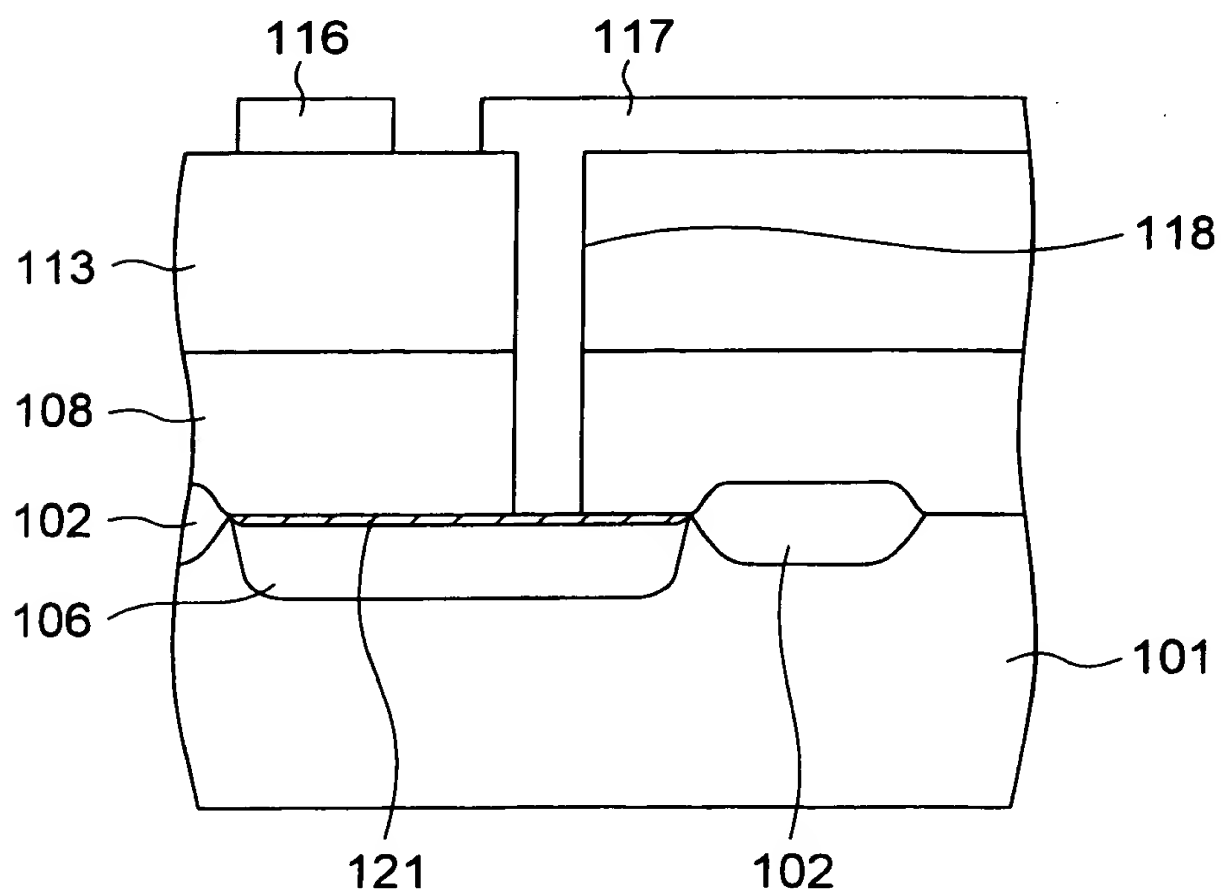


FIG. 2B b-b' SECTION

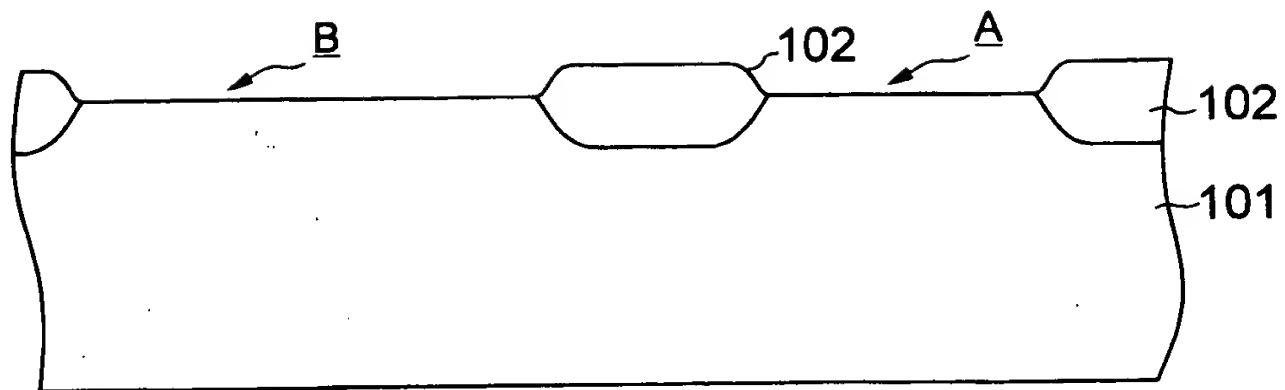


FIG. 3

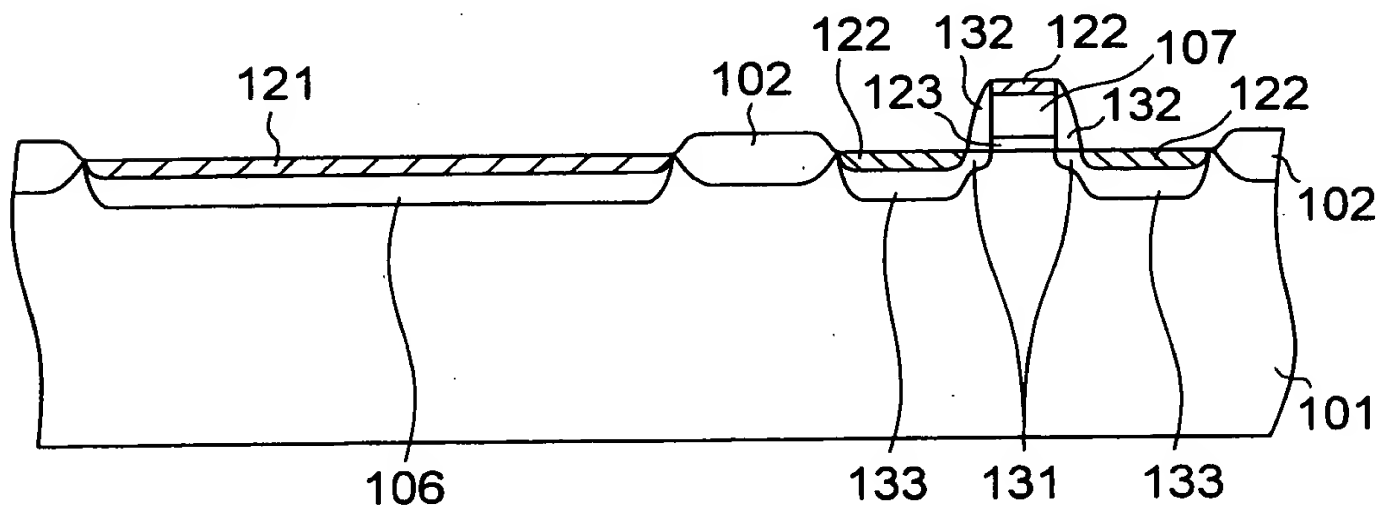


FIG. 4

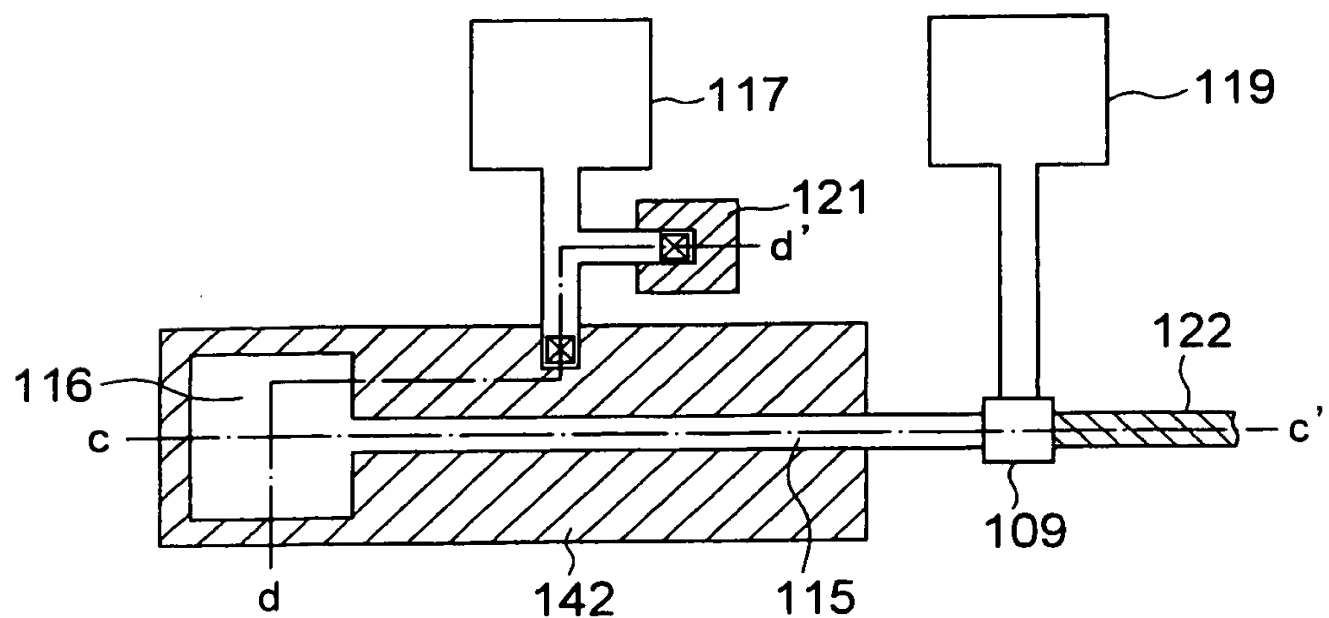


FIG. 5

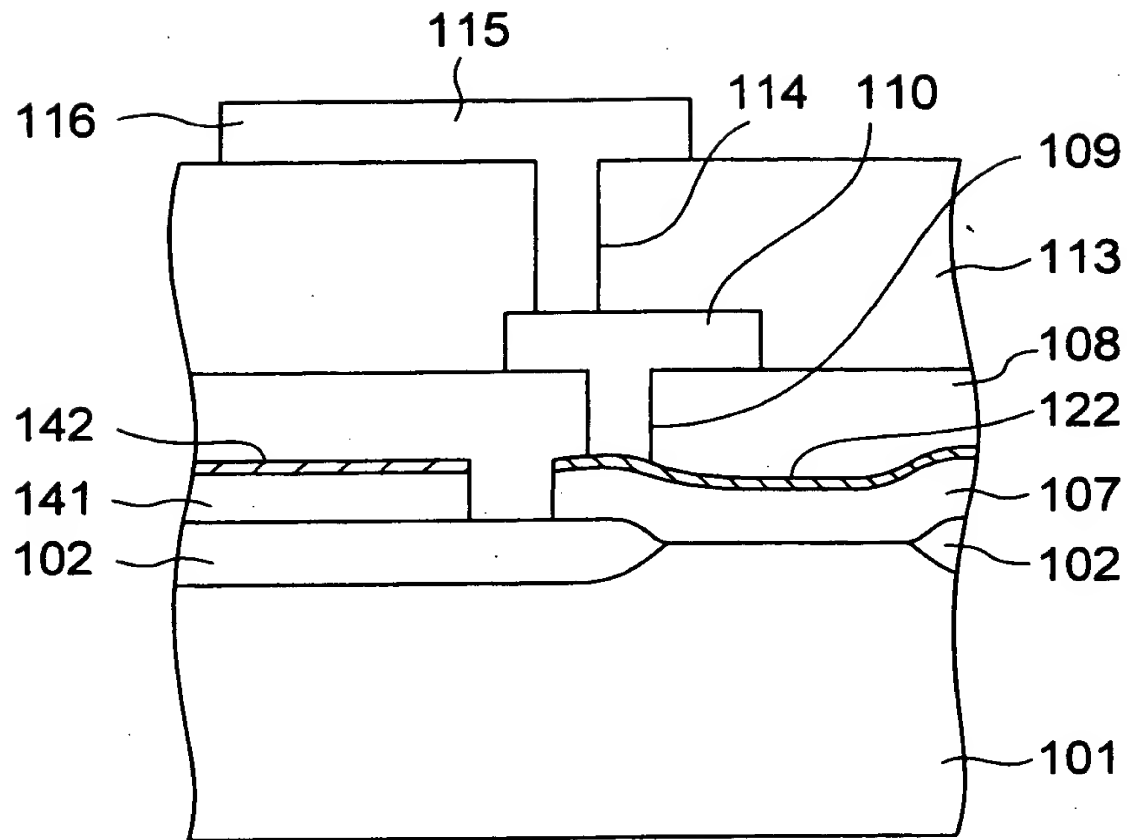


FIG. 6A c-c' SECTION

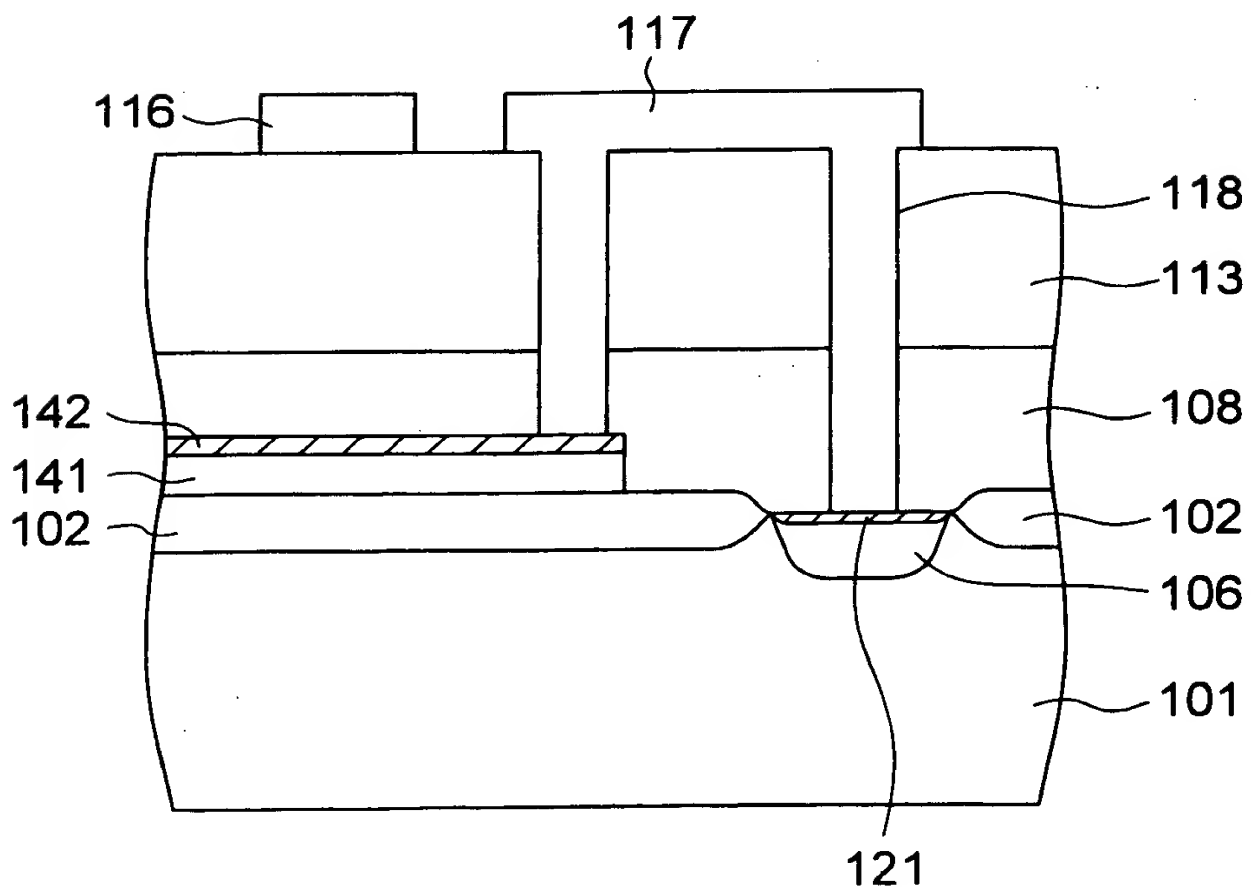
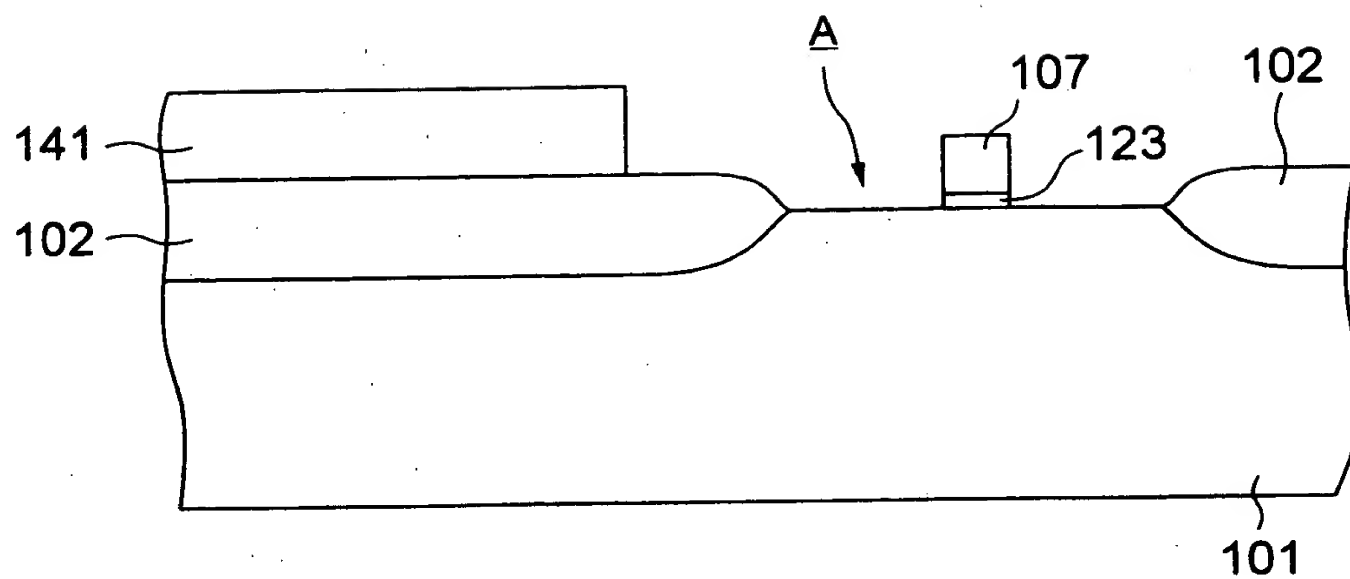
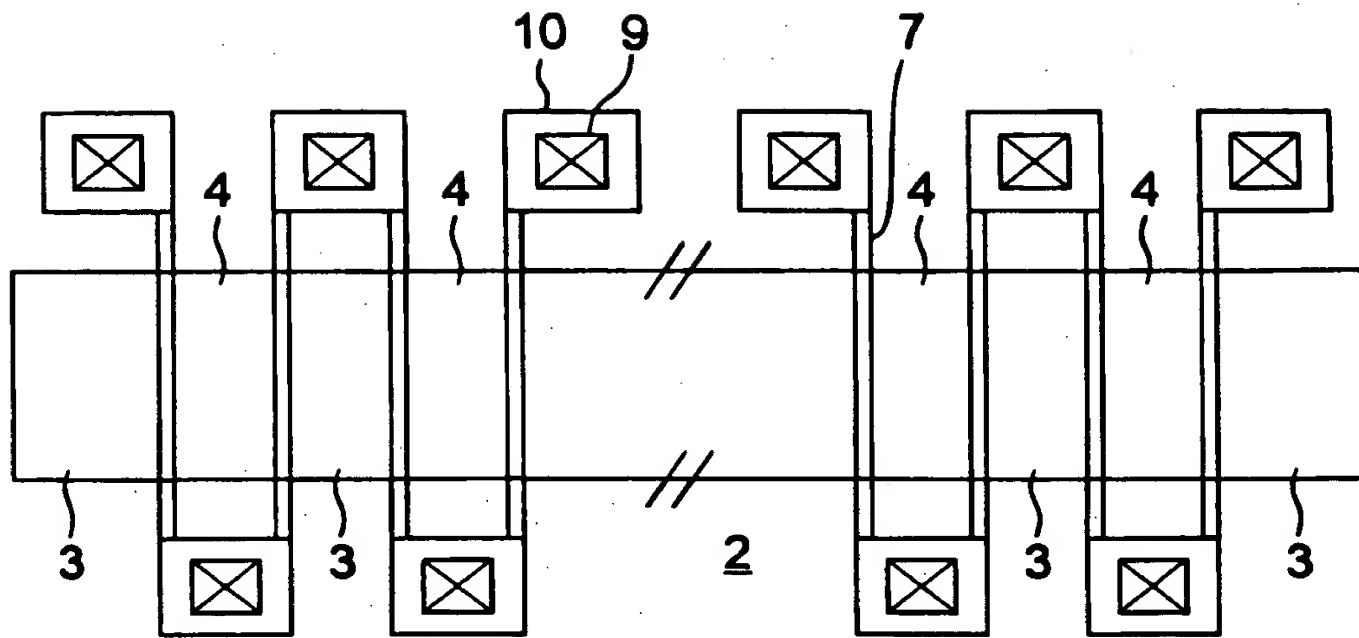


FIG. 6B d-d' SECTION

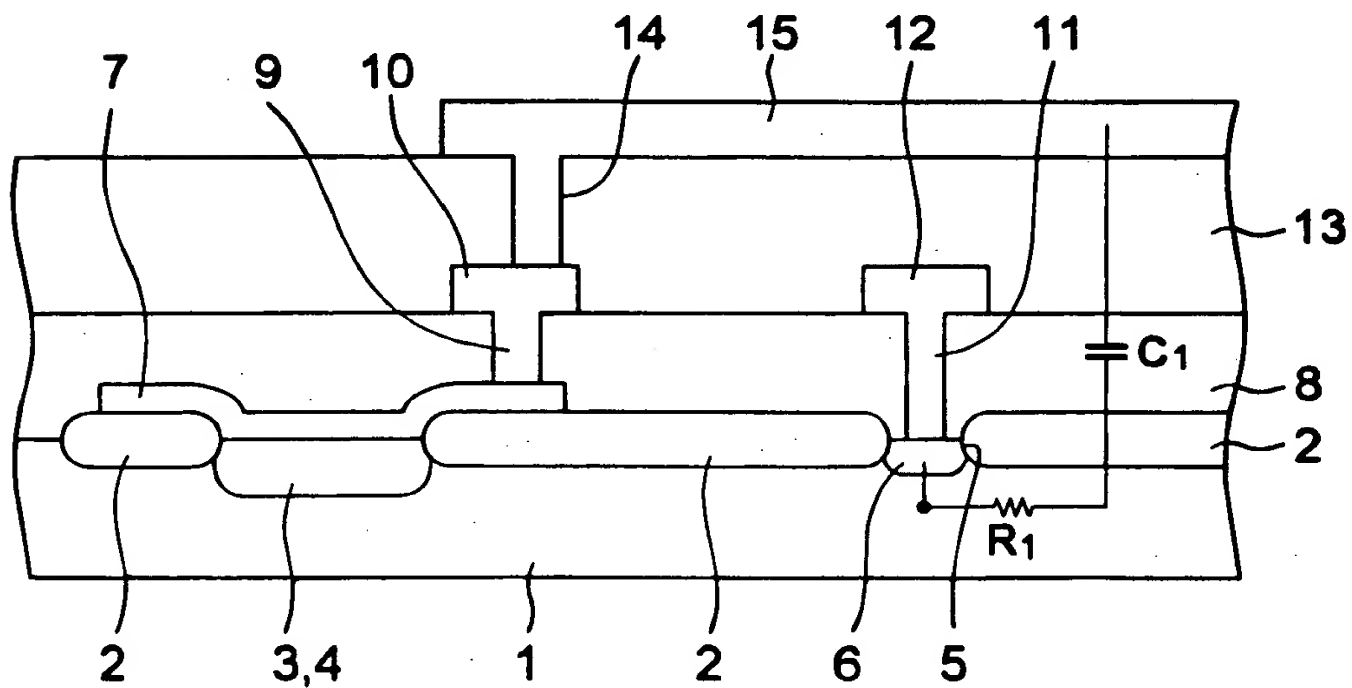


This cross-sectional view shows a semiconductor device with a central gate structure. The device consists of a substrate 101 with a top layer 102. A central gate stack is formed, including a gate dielectric 122, a gate core 107, and a gate cap 132. The gate is flanked by source/drain regions 123, which are covered by a layer 133. A side contact 141 is formed on the left side of the device, with a top layer 142. The bottom of the device is labeled 101.

FIG. 8



**FIG. 9**  
 (PRIOR ART)



**FIG. 10**  
 (PRIOR ART)

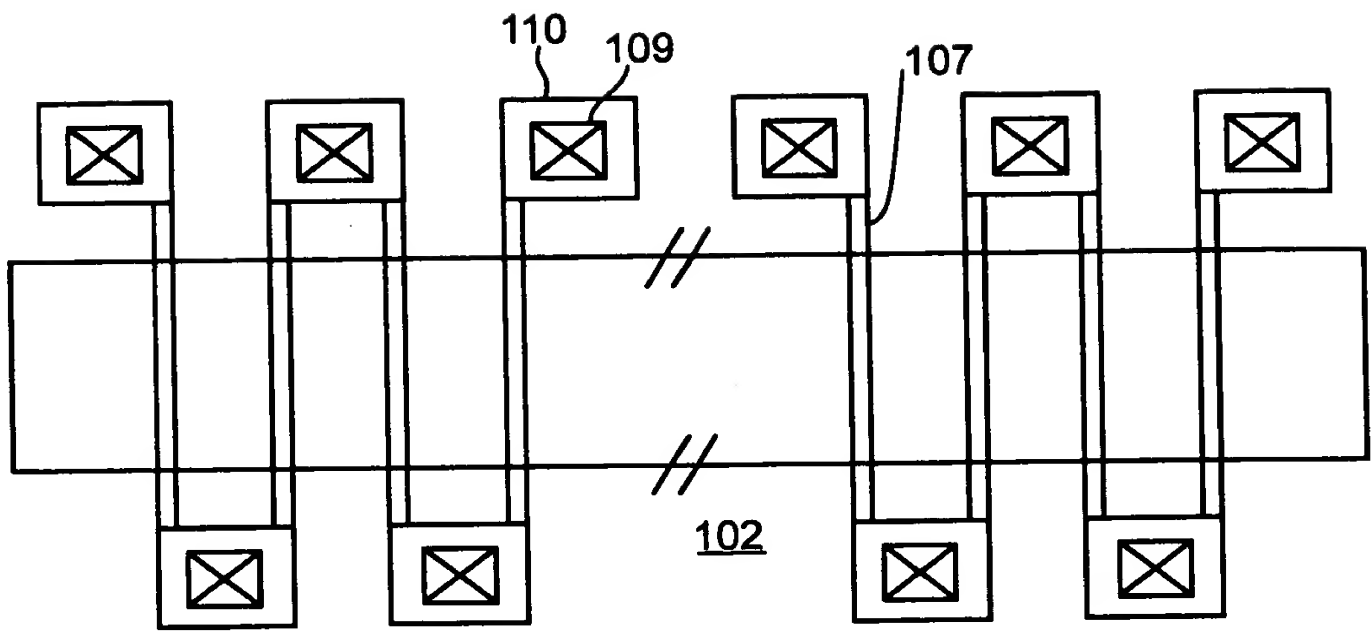


FIG. 11